

FIG. 2

FIG. 3

BITS 0-4 COUNTING ENABLES	BIT 5 INTERRUPT ENABLE	BITS 6-15	BIT 16 PMC2 INTERRUPT CONTROL	BIT 17 PMC2 INTERRUPT CONTROL	BIT 18 PMC2 COUNT CONTROL	BITS 19-25 PMC1 EVENT SELECTION	BITS 26-31 PMC2 EVENT SELECTION
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MONITOR MODE CONTROL REGISTER
(MMCR)

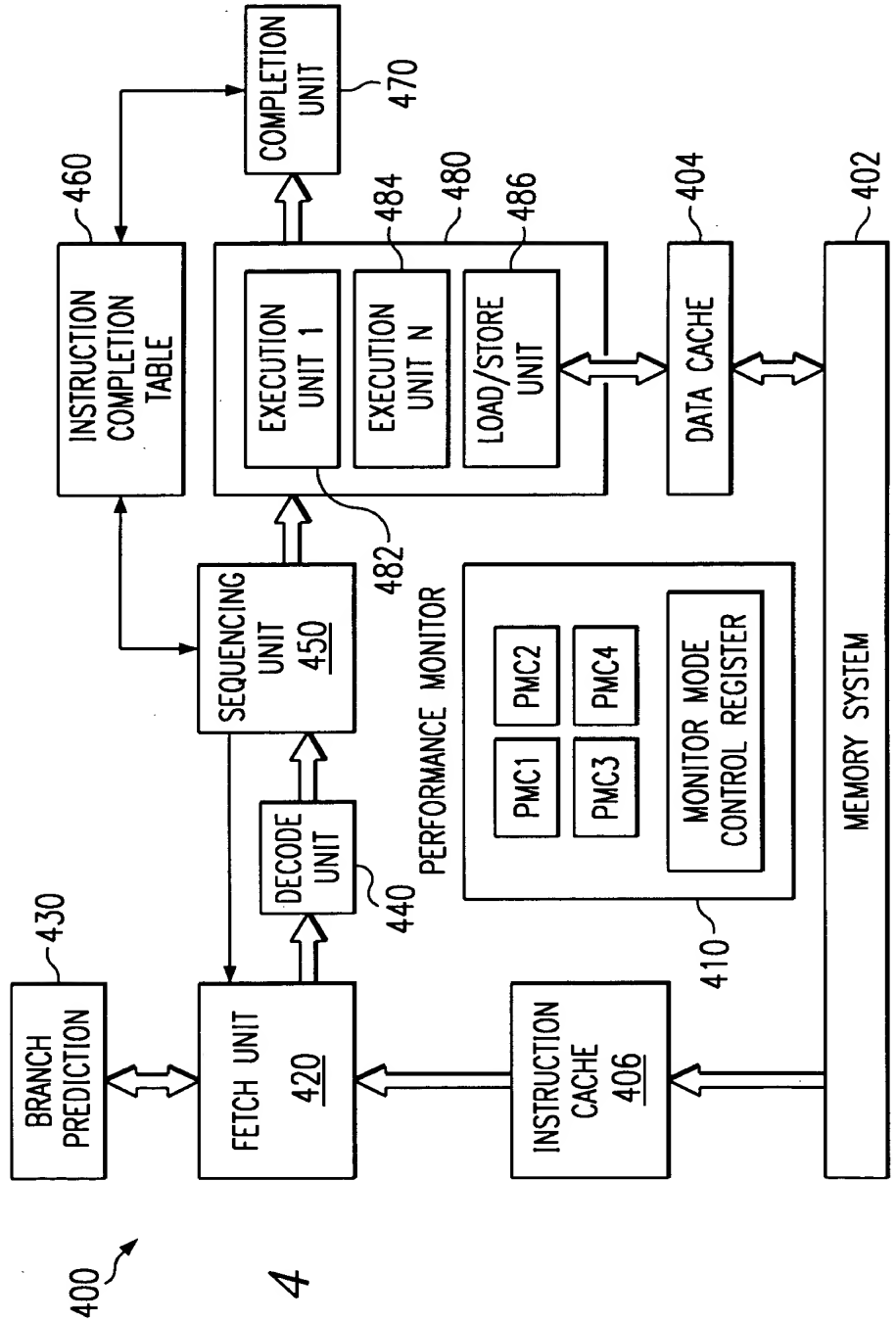


FIG. 4

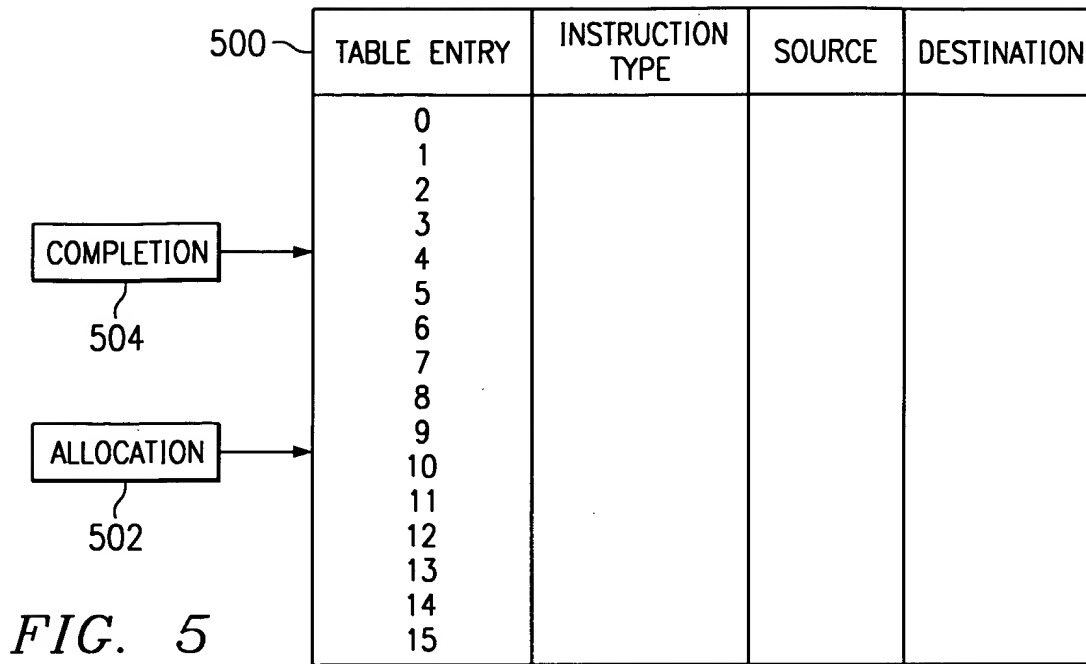


FIG. 5

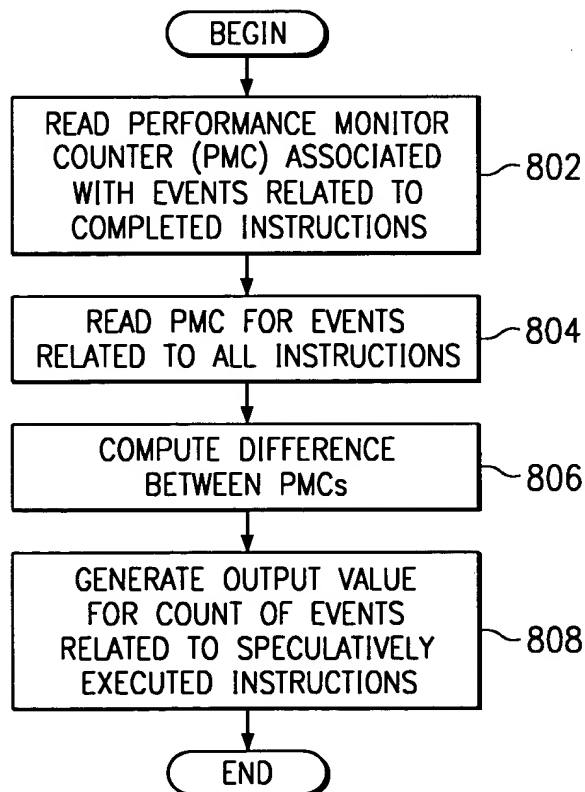


FIG. 8

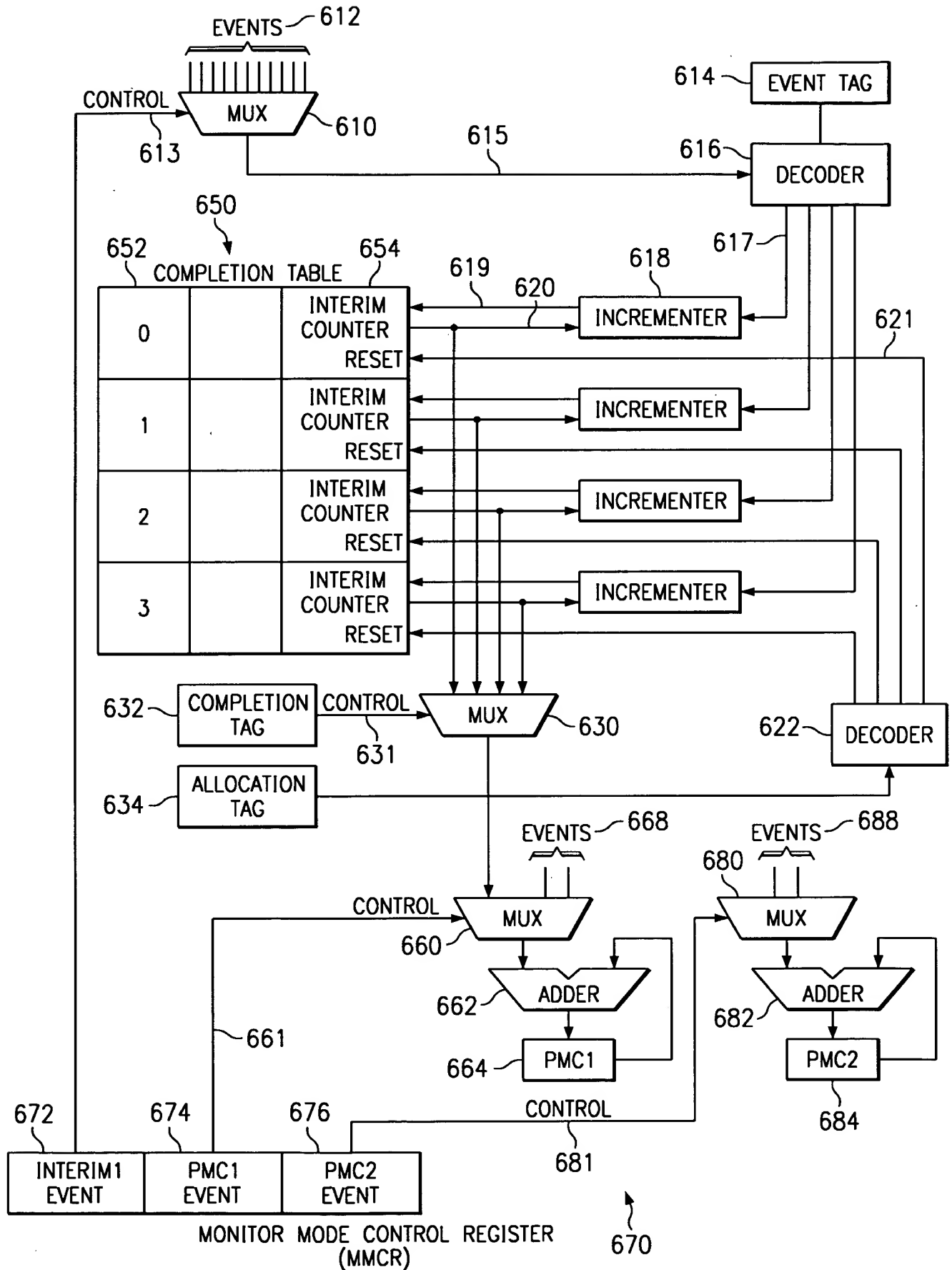


FIG. 6

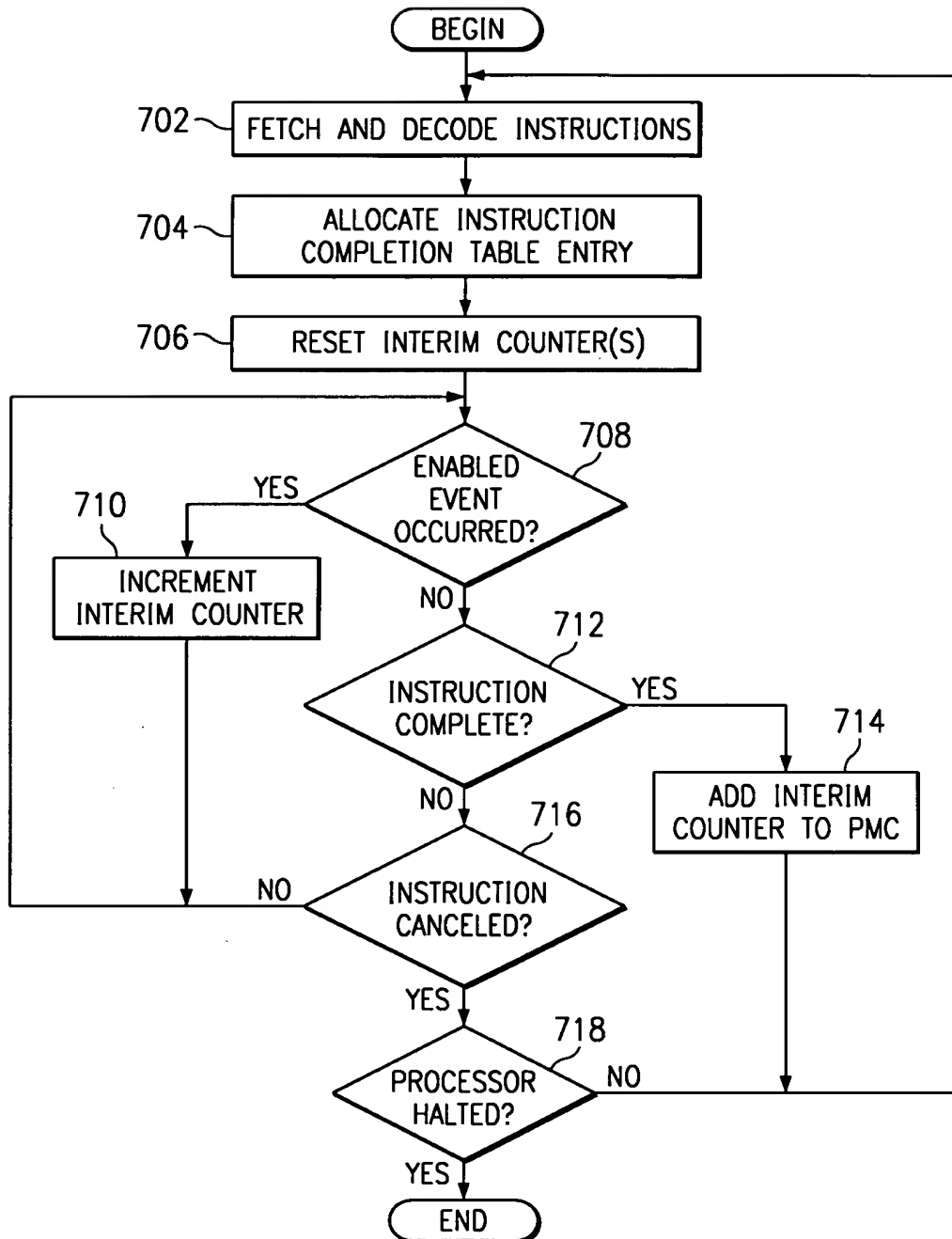


FIG. 7